**Date:** February 3rd

**From:** Adib Yahaya

**To:** Dr. Kaputa

**Subject:** Lab 1 PWM Module

**Introduction**

In this lab, I have created a pulse width modulation (PWM) module that can be used to control power supplied to electrical devices such as a motor. The reason for using PWM is because it is effective and simple to be implemented on an FPGA. To prove this, I have written the PWM module using VHDL and simulated the design using ModelSim. This design allows for flexible frequency and duty cycle. The PWM output can be enabled or disabled anytime by using the ‘enable’ input.

**Analysis**

This PWM module runs at 8 kHz frequency. The input clock speed is assumed to be 100 MHz. With 8 kHz frequency, the bit-resolution of the period and duty cycle are calculated to be 14 bits. Instead of using time as the basis for the period, I am using the number of clocks to calculate the duty cycle required for the modulation.

The backbone of this module is its counter. The counter can count up to 16383, which is the maximum value of a 14-bit counter. This is also the maximum number of clocks for the period and duty cycle. But for an 8 kHz PWM module, the period is set to 12500 clocks. This means that it takes 12500 clocks to complete one period (125 microsecond).

The duty cycle determines how long a PWM pulse will stay ‘on’ or ‘off’. This is done by having the module to output a ‘0’ every time the counter’s value exceed the duty cycle’s. A ‘1’ is produced only when the counter exceeds the period’s value. This means that a 0% duty cycle outputs a continuous low signal or ‘off’, meanwhile a 100% duty cycle outputs a continuous high signal or ‘on’.

**Conclusion**

* This module can accept any PWM frequency as long as the maximum number of clocks do not exceed 14-bits, though this limit can be easily changed in the source code.
* The duty cycle can be changed at any time which allows for quick changes and flexibility.
* An ‘enable’ input allows the PWM output to be enabled or disabled quickly.
* A high signal is produced at ‘error’ output port if the module was set up with incompatible period or duty cycle. No PWM output is produced either. Module has to be reset to restore normal operation.